IN THE CLAIMS:

Please cancel claims 1-10, 16, 18 and 19, and amend the claims as follows:

1-10. (Canceled)

11. (Currently Amended) ~~The method of claim 10, further comprising:~~ A method for selectively refreshing rows of memory cells in one or more semiconductor memory devices, comprising:

monitoring, by a memory controller coupled with the semiconductor memory devices, write operations to the memory cells;

maintaining a plurality of bits indicative of rows containing memory cells involved in the monitored write operations on the memory controller;

transferring a first plurality of the bits to a first memory device; and

placing the first memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the first plurality of bits.

12. (Original) The method of claim 11, further comprising:

transferring a second plurality of the bits to a second memory device; and

placing the second memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the second plurality of bits.

13. (Currently Amended) A semiconductor memory device, comprising:

a plurality of rows of memory cells;

refresh circuitry configured to issue refresh requests for the rows of memory cells when the memory device is placed in a self-refresh mode;

row state circuitry configured to maintain a plurality of bits indicative of rows that are to be refreshed;

interface circuitry configured to receive the plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry; and

refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry.

14. (Original) The semiconductor memory device of claim 13, wherein the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued by generating a signal used to inhibit refresh requests.

15. (Original) The semiconductor memory device of claim 14, wherein the signal is generated by accessing a bit corresponding to a row address generated by a refresh address counter.

16. (Canceled)

17. (Currently Amended) The semiconductor memory device of claim ~~16~~ 15, wherein each bit corresponds to a single row of memory cells.

18. (Canceled)

19. (Canceled)

20. (Original) A system, comprising:

a memory device having a plurality of rows of memory cells, wherein the memory device is configured to limit the number of rows that are refreshed, during a self-refresh mode, based on row data indicative of rows that are to be refreshed; and

a memory controller configured to monitor write operations to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self-refresh mode.

21. (Original) The system of claim 20, wherein:

the row data is stored in the memory device in an array of memory cells; and

the memory controller is further configured to reset the array of memory cells prior to transferring the row data to the memory device.

22. (Original) The system of claim 21, wherein the memory controller is configured to reset the array of memory cells by writing to a mode register of the memory device.

23. (Original) The system of claim 20, wherein the memory controller is configured to set a bit in the row data to indicate one or more cells in a corresponding row have been written.